

# EE 505

## Lecture 12

### DAC Design

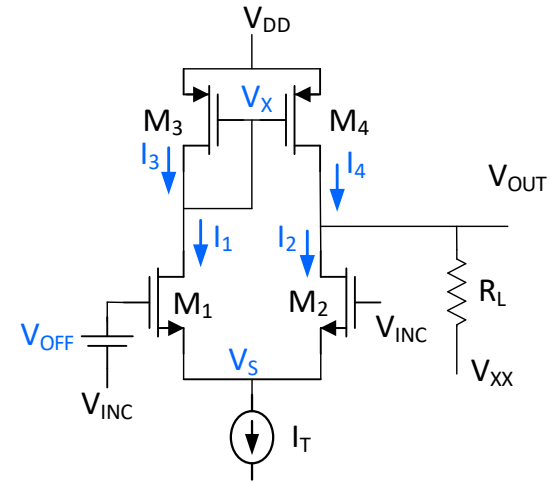
- DAC Architectures
- String DACs

## Review from Last Lecture

### Analysis of Offset Voltage

but

$$\sigma_{V_T}^2 = \frac{A_{VT0}^2}{WL} \quad \sigma_{\frac{\mu_R}{\mu_N}}^2 = \frac{A_{\mu}^2}{WL} \quad \sigma_{\frac{C_{OXR}}{C_{OXN}}}^2 = \frac{A_{Cox}^2}{WL} \quad \sigma_{\frac{L_R}{L_N}}^2 = \frac{2A_L^2}{WL^2} \quad \sigma_{\frac{W_R}{W_N}}^2 = \frac{2A_W^2}{W^2L}$$



So the offset variance can be expressed as

$$\sigma_{V_{OFF}}^2 = 2 \frac{A_{VTn0}^2}{W_1 L_1} + 2 \frac{\mu_p L_1}{\mu_n W_1} \frac{A_{VTp0}^2}{L_3^2} + V_{EB3}^2 \frac{\mu_p L_1 W_3}{\mu_n L_3 W_1} \frac{1}{2} \left[ \frac{A_{\mu_n}^2}{W_3 L_3} + \frac{A_{\mu_p}^2}{W_1 L_1} + A_{Cox}^2 \left( \frac{1}{W_3 L_3} + \frac{1}{W_1 L_1} \right) + A_W^2 \left( \frac{2}{W_3^2 L_3} + \frac{2}{W_1^2 L_1} \right) + A_L^2 \left( \frac{2}{W_1 L_1^2} + \frac{2}{W_3 L_3^2} \right) \right]$$

Often this can be approximated by

$$\sigma_{V_{OFF}}^2 = 2 \frac{A_{VTn0}^2}{W_1 L_1} + 2 \frac{\mu_p L_1}{\mu_n W_1} \frac{A_{VTp0}^2}{L_3^2} + V_{EB3}^2 \frac{\mu_p L_1 W_3}{\mu_n L_3 W_1} \frac{1}{2} \left[ \frac{A_{\mu_n}^2}{W_3 L_3} + \frac{A_{\mu_p}^2}{W_1 L_1} + A_{Cox}^2 \left( \frac{1}{W_3 L_3} + \frac{1}{W_1 L_1} \right) \right]$$

Or even approximated by

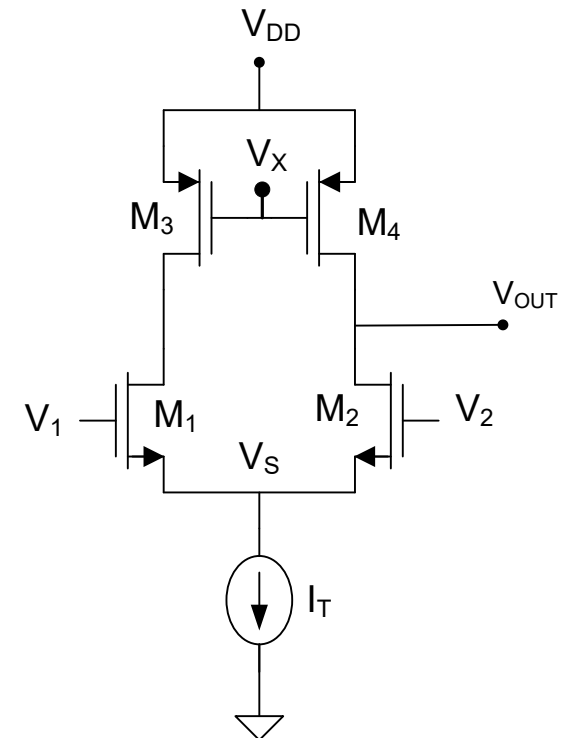
$$\sigma_{V_{OFF}}^2 = 2 \frac{A_{VTn0}^2}{W_1 L_1} + 2 \frac{\mu_p L_1}{\mu_n W_1} \frac{A_{VTp0}^2}{L_3^2}$$

# Correspondingly: Random Offset Voltages

$$\sigma_{V_{os}}^2 = 2 \left[ \frac{A_{V_{TO n}}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{V_{TO p}}^2 + \frac{V_{EBn}^2}{4} \left( \frac{1}{W_n L_n} A_{\mu_n}^2 + \frac{1}{W_p L_p} A_{\mu_p}^2 + A_{COX}^2 \left[ \frac{1}{W_n L_n} + \frac{1}{W_p L_p} \right] \right) \right. \\ \left. + 2A_L^2 \left[ \frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2} \right] + A_w^2 \left[ \frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2} \right] \right]$$

which again simplifies to

$$\sigma_{V_{os}}^2 \cong 2 \left[ \frac{A_{V_{TO n}}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{V_{TO p}}^2 \right]$$



Note these offset voltage expressions are identical!

# Random Offset Voltages

Example: Determine the  $3\sigma$  value of the input offset voltage for

The MOS differential amplifier is

a)  $M_1$  and  $M_3$  are minimum-sized and

b) the area of  $M_1$  and  $M_3$  are 100 times minimum size

$$\sigma_{V_{os}}^2 \cong 2 \left[ \frac{A_{VTO n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTO p}^2 \right]$$

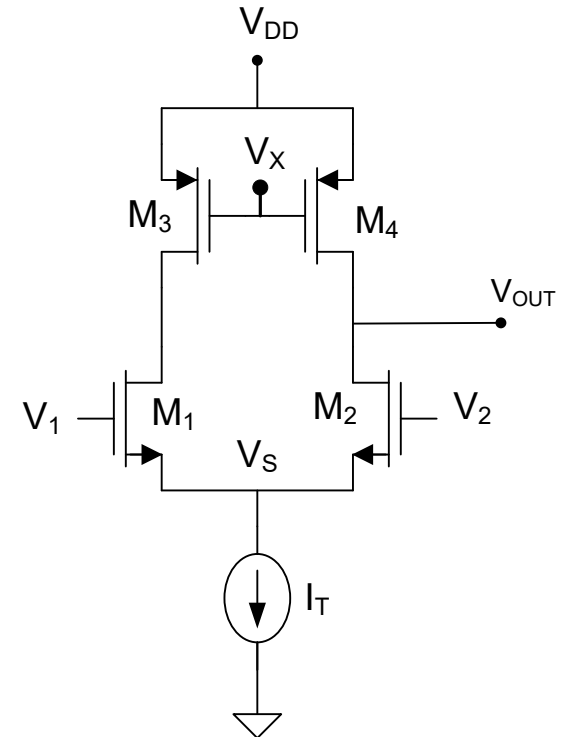
$$\sigma_{V_{os}}^2 \cong \frac{2}{W_n L_n} \left[ A_{VTO n}^2 + \frac{\mu_p}{\mu_n} A_{VTO p}^2 \right]$$

a)

$$\sigma_{V_{os}}^2 \cong \frac{2}{(0.5\mu)^2} \left[ .021^2 + \frac{1}{3} .025^2 \right]$$

$$\sigma_{V_{os}} \cong 72\text{mV}$$

$$3 \sigma_{V_{os}} \cong 216\text{mV}$$



Note this is a very large offset voltage !

# Random Offset Voltages

Example: Determine the  $3\sigma$  value of the input offset voltage for

The MOS differential amplifier is

a)  $M_1$  and  $M_3$  are minimum-sized and

b) the area of  $M_1$  and  $M_3$  are 100 times minimum size

$$\sigma_{V_{os}}^2 \cong 2 \left[ \frac{A_{VTO n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTO p}^2 \right]$$

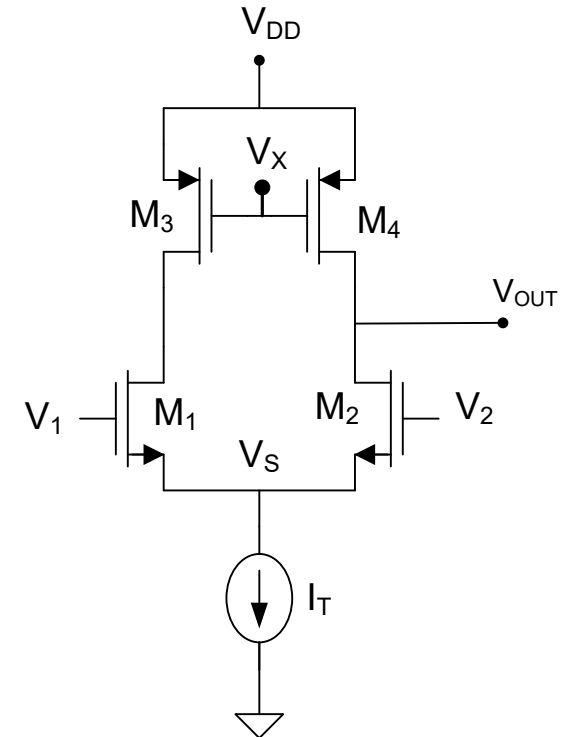
$$\sigma_{V_{os}}^2 \cong \frac{2}{W_n L_n} \left[ A_{VTO n}^2 + \frac{\mu_p}{\mu_n} A_{VTO p}^2 \right]$$

b)

$$\sigma_{V_{os}}^2 \cong \frac{2}{100(0.5\mu)^2} \left[ .021^2 + \frac{1}{3} .025^2 \right]$$

$$\sigma_{V_{os}} \cong 7.2\text{mV}$$

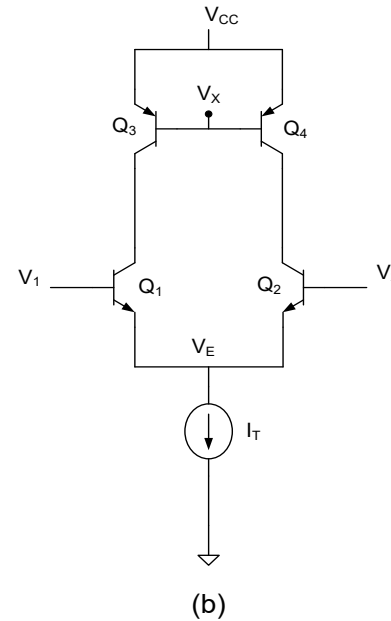
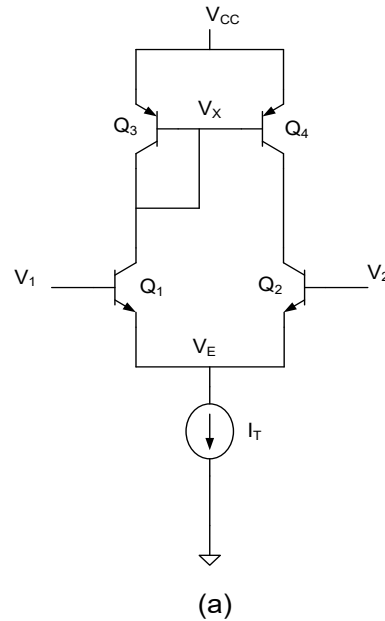
$$3 \sigma_{V_{os}} \cong 21.6\text{mV}$$



Note this is much lower but still a large offset voltage !

The area of  $M_1$  and  $M_3$  needs to be very large to achieve a low offset voltage

# Random Offset Voltages



It can be shown that

$$\sigma_{V_{os}}^2 \cong 2V_t^2 \left[ \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right]$$

where very approximately

$$A_{Jn} = A_{Jp} = 0.1\mu$$

# Random Offset Voltages

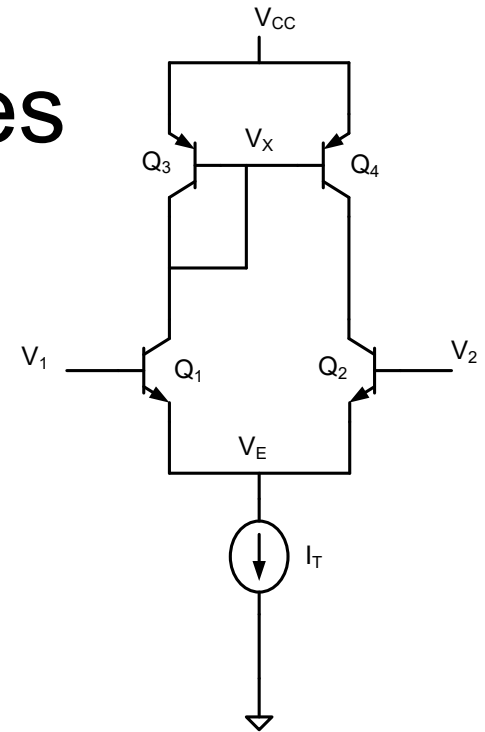
Example: Determine the  $3\sigma$  value of the offset voltage of a the bipolar input stage if  $A_{E1}=A_{E3}=10\mu^2$

$$\sigma_{V_{os}}^2 \cong 2V_t^2 \left[ \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right]$$

$$\sigma_{V_{os}} \cong \sqrt{2}V_t A_J \frac{\sqrt{2}}{\sqrt{A_E}}$$

$$\sigma_{V_{os}} \cong 2 \bullet 25\text{mV} \bullet 0.1\mu \bullet \frac{1}{\sqrt{10\mu^2}} = 1.6\text{mV}$$

$$3\sigma_{V_{os}} \cong 4.7\text{mV}$$



Note this value is much smaller than that for the MOS input structure !

# Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50mV

BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

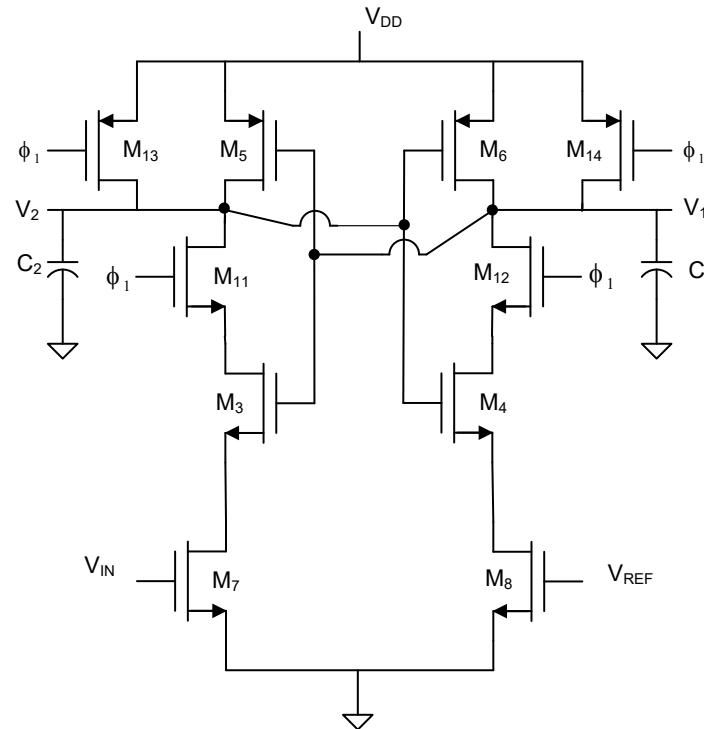
Often more practical to include offset-compensation circuitry



## Review from Last Lecture

## Dynamic Comparators (Regenerative)

Offset voltage difficult to determine in some classes of comparators



## Dynamic clocked comparator

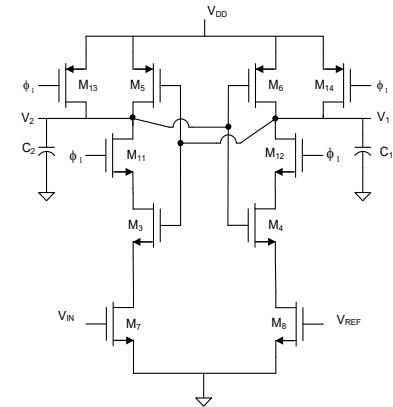
- When  $\phi_1$  is low,  $V_1$  and  $V_2$  are precharged to  $V_{DD}$  and no static power is dissipated
- When  $\phi_1$  is high, enters evaluate state and no static power is dissipated
- Power dissipation almost entirely associated with charging and discharging parasitic capacitors

## Review from Last Lecture

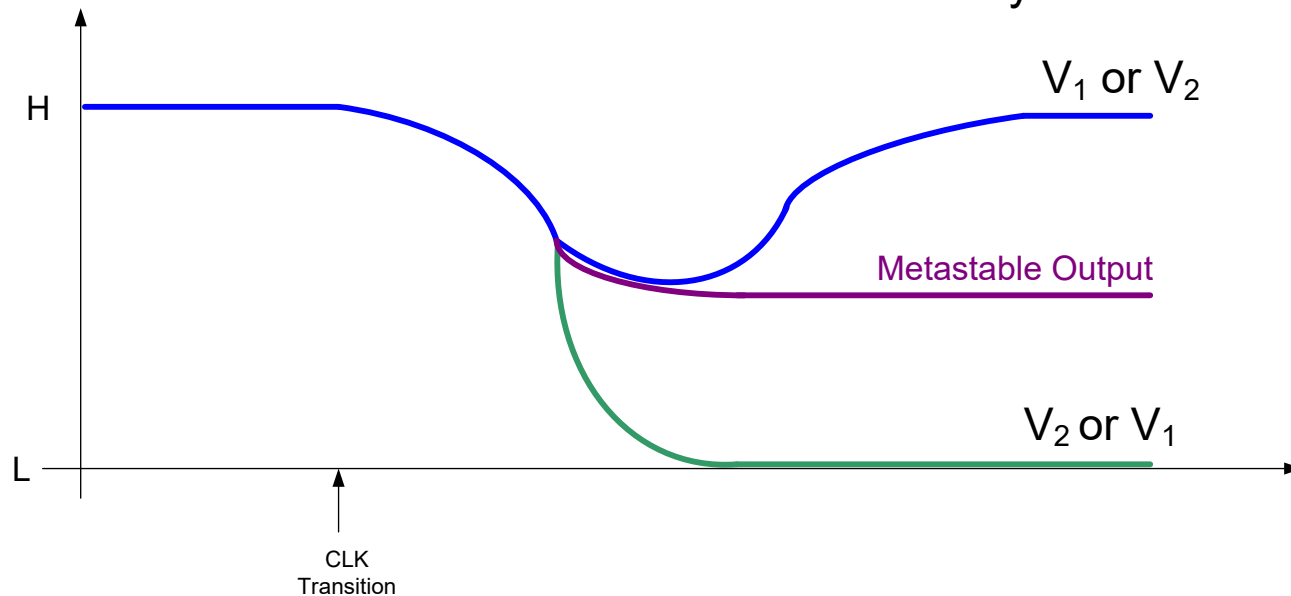
Offset voltage difficult to determine in some classes of comparators

Very small, very fast, low power

But offset voltage can be large (100mV or more)

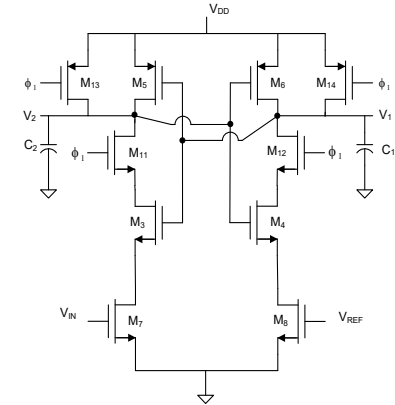
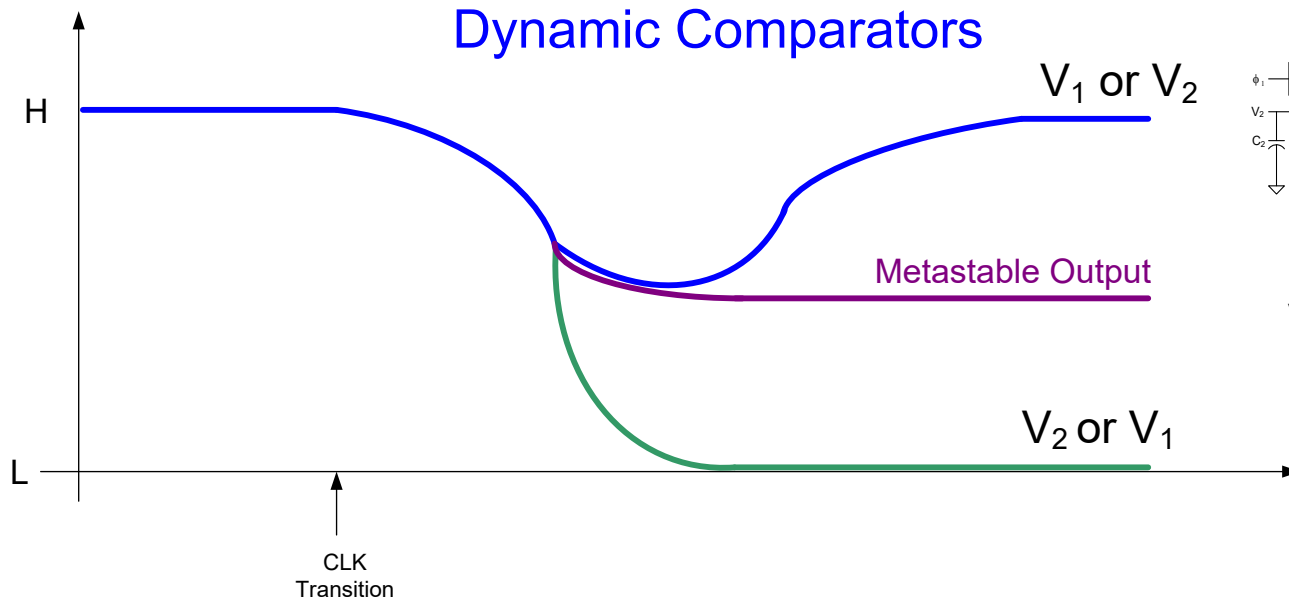


Dynamic clocked comparator



Decision is being made shortly after clock transition when devices are deep in weak inversion and signal levels are very small

### Dynamic Comparators



Dynamic Comparators widely used because of low power dissipation

Often include one or more pre-amp stages before regeneration applied

Previous-code dependence and kickback both of concern in dynamic comparators

Noise may significantly affect performance and difficult to analyze and simulate because transient noise models in deep weak inversion are questionable

Still major opportunities to make significant improvement in dynamic comparators

# Summary of Offset Voltage Issues

- Random offset voltage is generally dominant and due to mismatch in device and model parameters
- MOS Devices have large  $V_{OS}$  if area is small
- $\sigma$  decreases approximately with  $1/\sqrt{A}$
- Multiple fingers for MOS devices offer benefits for common centroid layouts but too many fingers will ultimately degrade offset because perimeter/area ratio will increase ( $A_W$  and  $A_L$  will become of concern)
- Offset voltage of dynamic comparators is often large and analysis not straightforward
- Offset compensation often used when low offsets important

MOS: 
$$\sigma_{V_{OS}}^2 \cong 2 \left[ \frac{A_{VTO n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTO p}^2 \right]$$

Bipolar: 
$$\sigma_{V_{OS}}^2 \cong 2V_t^2 \left[ \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right]$$

# DAC Architectures

## Types (Nyquist Rate)

- Voltage Scaling
  - Resistor String DACs (string DACs)
  - Interpolating
- Current Steering
  - Binary Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented
- Charge Redistribution
  - Switched Capacitor
- Serial
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined
- Integrating
- Resistor Switching
- MDACs (multiplying DACs)

# Observations

- Yield Loss is the major penalty for not appropriately managing parasitics and matching and this loss can be ruthless
- The ultimate performance limit of essentially all DACs is the yield loss associated with parasitics and matching
- Many designers do not have or use good statistical models that accurately predict data converter performance
- If you work of a company that does not have good statistical device models
  - Convince model groups of the importance of developing these models
  - (or) develop appropriate test structures to characterize your process
- Existing nonlinear device models may not sufficiently accurately predict device nonlinearities for high-end data converter applications

# DAC Architectures

## Structures

- Hybrid or Segmented
- Mode of Operation
  - Current Mode
  - Voltage Mode
  - Charge Mode
- Self-Calibrating
  - Analog Calibration
    - Foreground
    - Background
  - Digital Calibration
    - Foreground
    - Background
  - Dynamic Element Matching
- Laser or Link Trimmed
- Thermometer Coded or Binary
- Radix 2 or non-radix 2
- Inherently Monotone

# DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
    - Charge Redistribution
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored !
- Major challenge is in determining appropriate architecture and managing the parasitics



# Nonideal Effects of Concern

- Matching
- Parasitic Capacitances  
(including Charge injection)
- Loading
- Nonlinearities
- Interconnect resistors
- Noise
- Speed
- Jitter
- Temperature Effects
- Aging
- Package stress

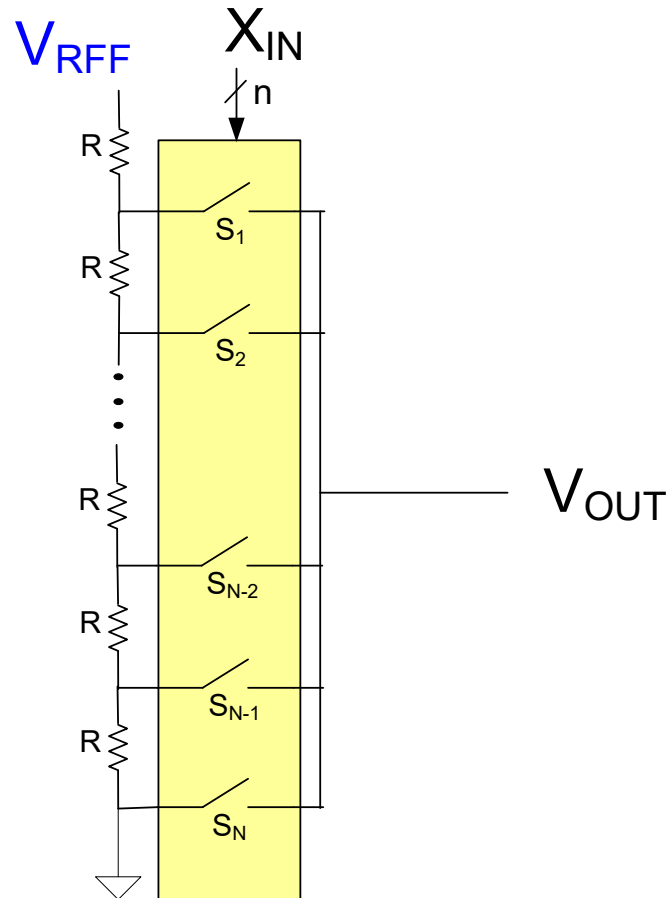
# Observations

- Experienced Designers/Companies often produce superior data converter products
- Essentially all companies have access to the same literature, regularly reverse engineer successful competitors products and key benefits in successful competitors products are generally not locked up in patents
- High-end designs( speed and resolution) may get attention in the peer community but practical moderate performance converters usually make the cash flow
- Area (from a silicon cost viewpoint) is usually not the driving factor in high-end designs where attractive price/mfg cost ratios are common
- Considerable ongoing demand for data converter designers – particularly in ASICs where DAC optimized for specific application

# DAC Architectures



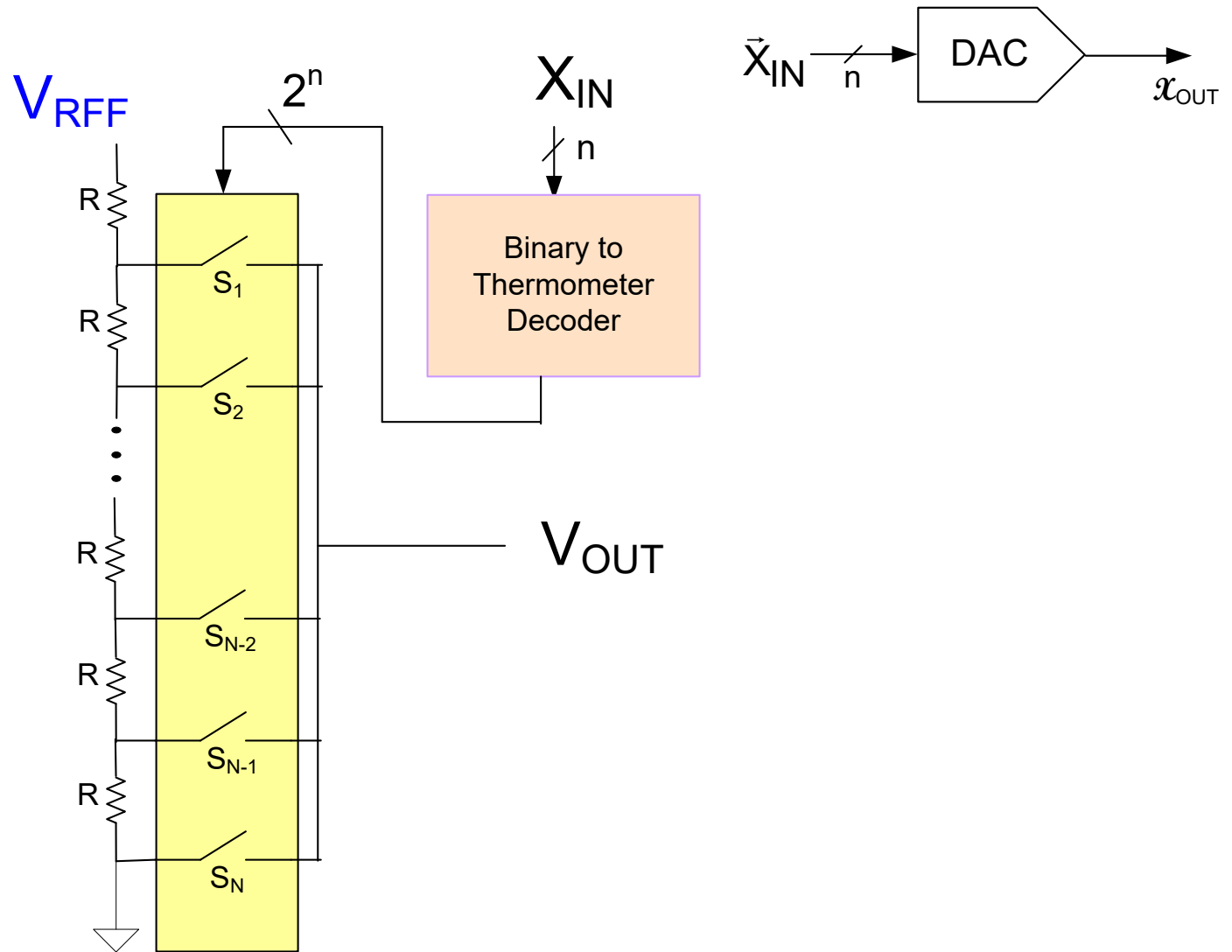
## R-String



$X_{IN}$  is decoded to close one switch

# DAC Architectures

## R-String

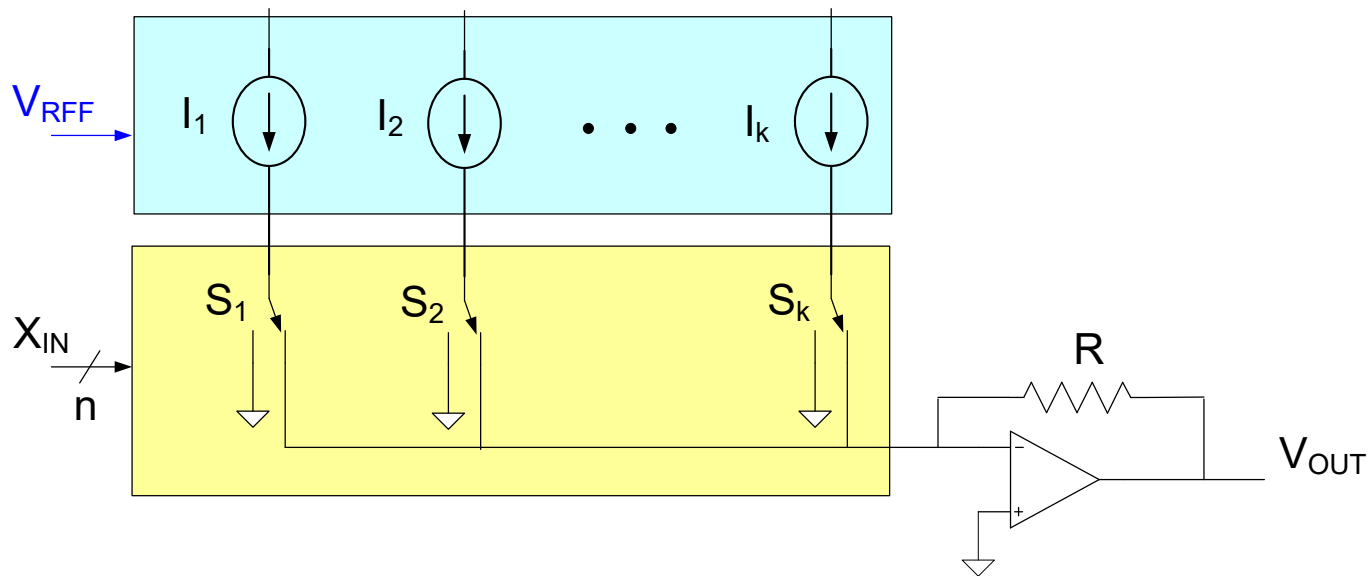


Basic R-String DAC including Logic to Control Switches

# DAC Architectures

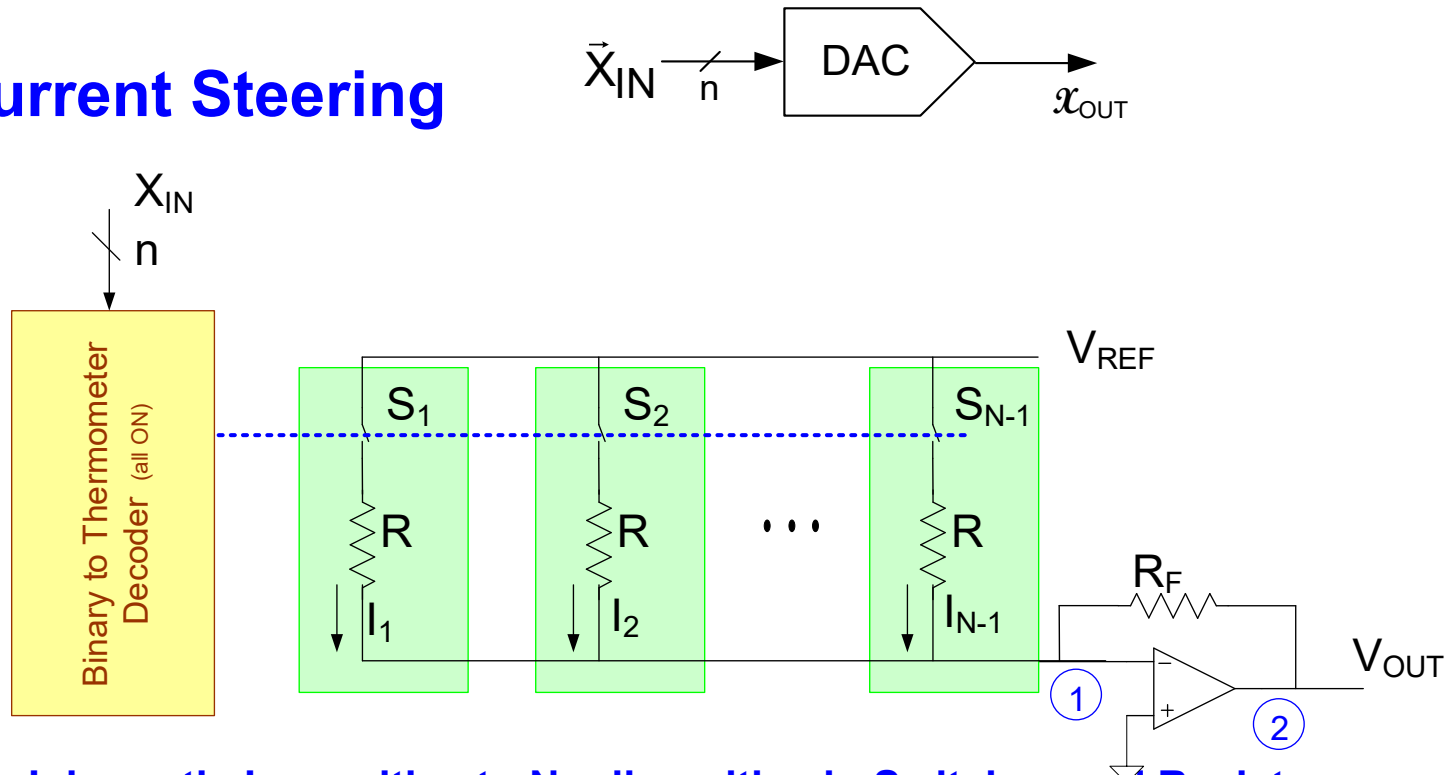


## Current Steering



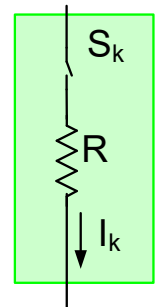
# DAC Architectures

## Current Steering



### Inherently Insensitive to Nonlinearities in Switches and Resistors

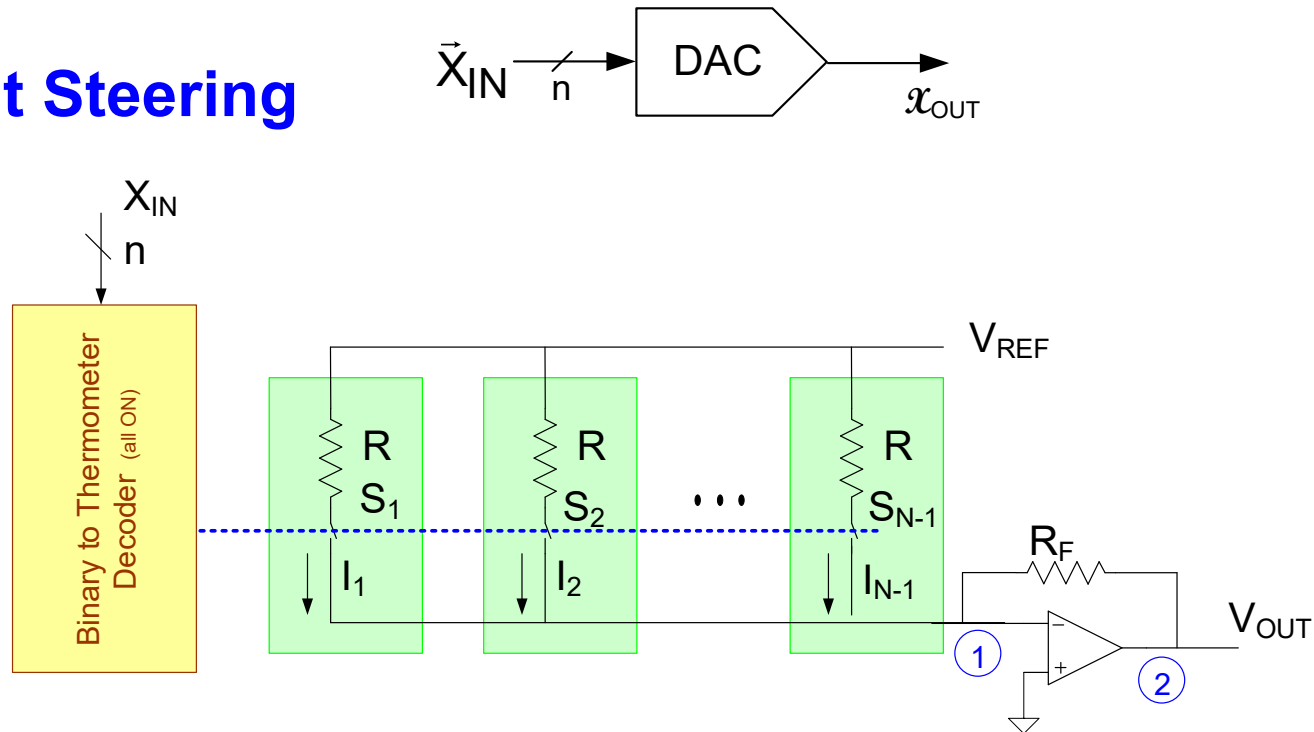
- Termed “top plate switching”
- Thermometer coded
- Based upon unary cell
- Speed limited by Op Amp and clock transients
- Device count becomes impractical for large  $N$



Unary bit cell

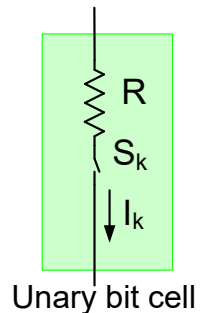
# DAC Architectures

## Current Steering



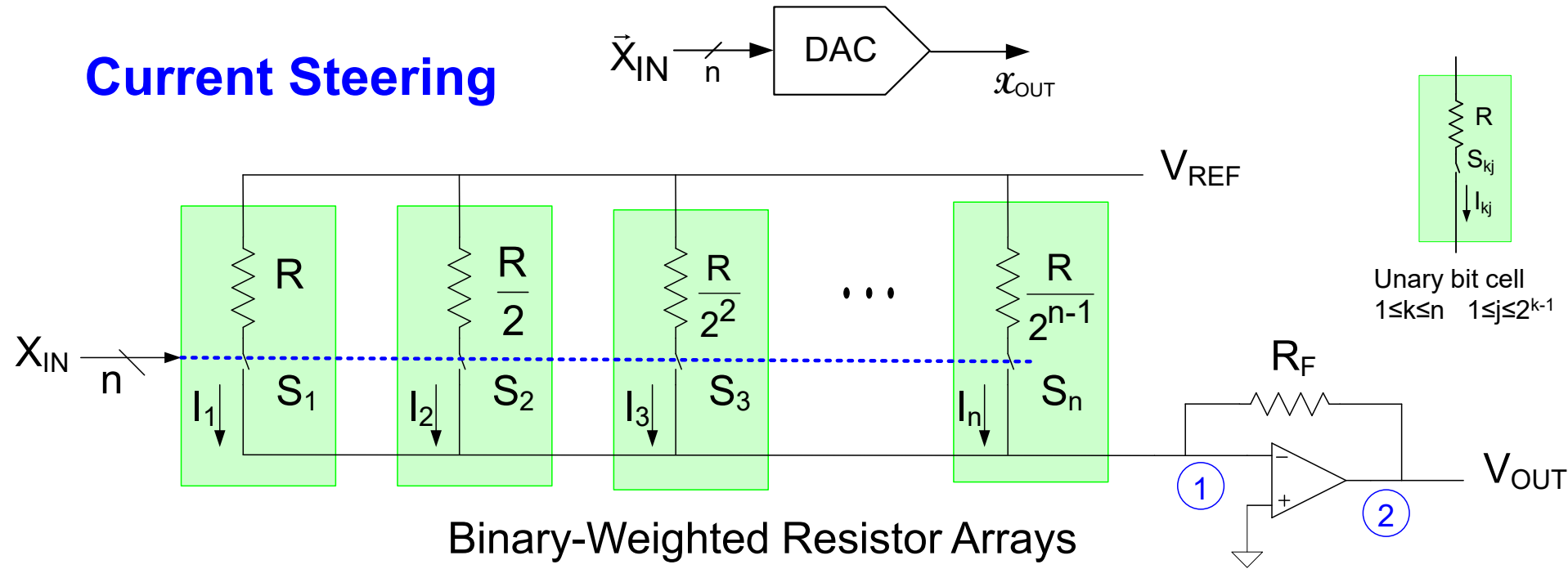
**Inherently Insensitive to Nonlinearities in Switches and Resistors**  
**Smaller ON resistance and less phase-shift from clock edges**

- Termed “bottom plate switching”
- Thermometer coded
- Based upon unary cell
- Speed limited by Op Amp
- Device count becomes impractical for large  $N$



# DAC Architectures

## Current Steering



## Binary-Weighted Resistor Arrays

- Unary bit cells usually bundled to make resistors
- Same number of unary cells needed as for thermometer coded structure
- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical

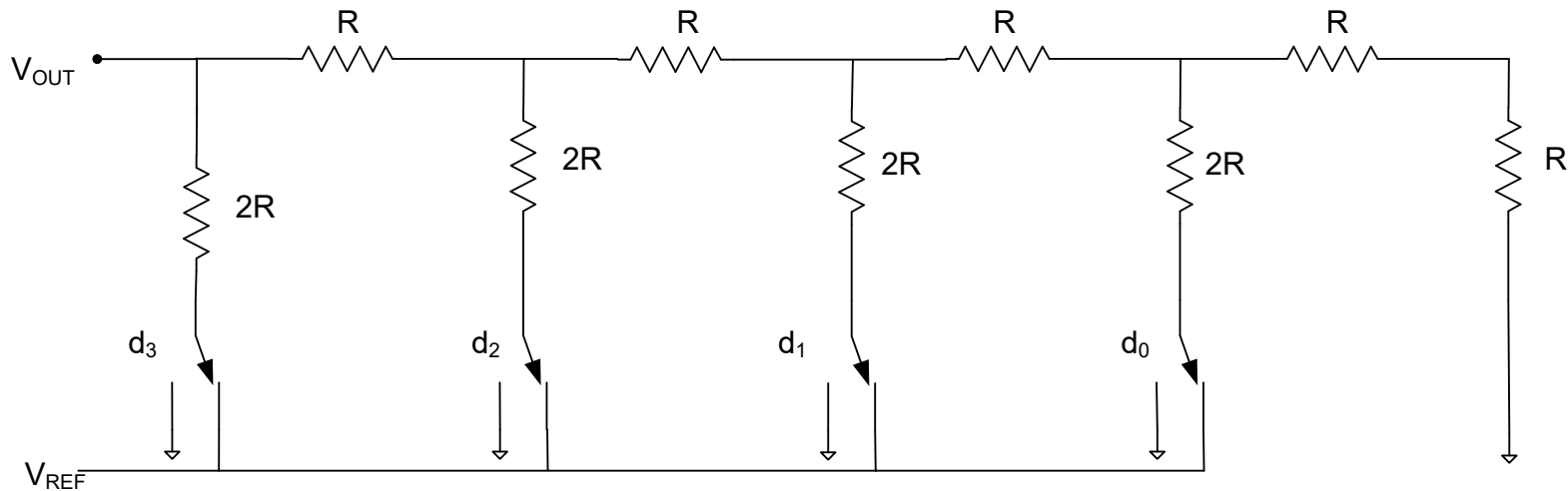
Observe thermometer coding and binary weighted both offer some major advantages and some major limitations



# DAC Architectures



**R-2R** (one variant) (4-bits shown)



By superposition:

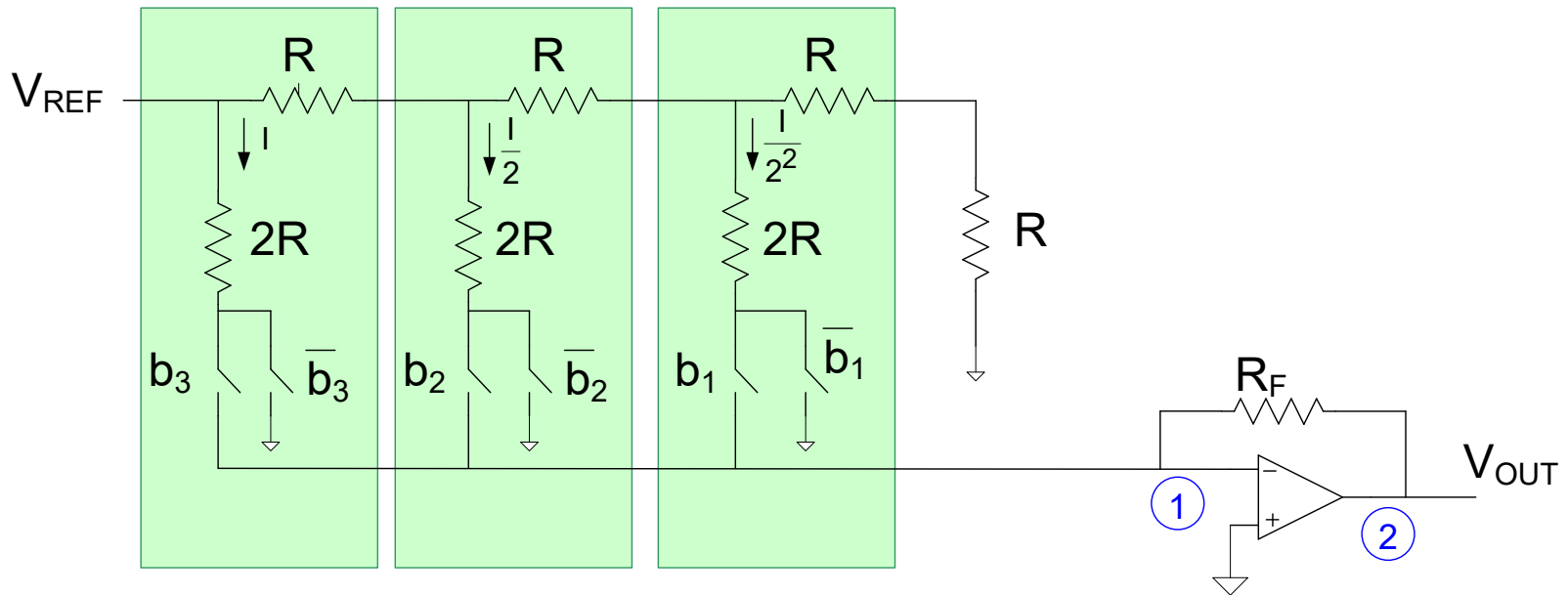
$$V_{OUT} = V_{REF} d_3 \cdot \frac{1}{2} + V_{REF} d_2 \cdot \frac{1}{4} + V_{REF} d_1 \cdot \frac{1}{8} + V_{REF} d_0 \cdot \frac{1}{16} = V_{REF} \sum_{k=0}^3 \frac{d_k}{2^{4-k}} = V_{REF} \sum_{k=1}^4 \frac{d_{4-k}}{2^k}$$

# DAC Architectures

## Current Steering



## R-2R (another variant)

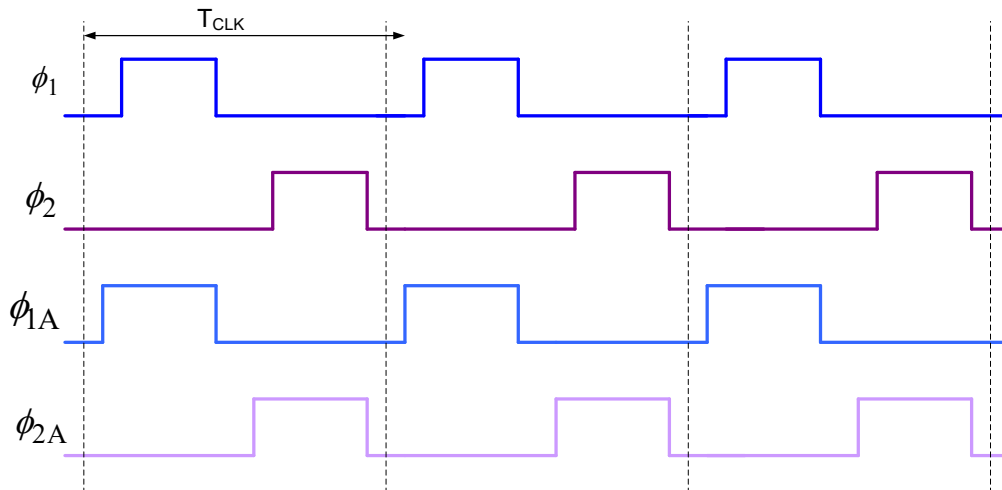
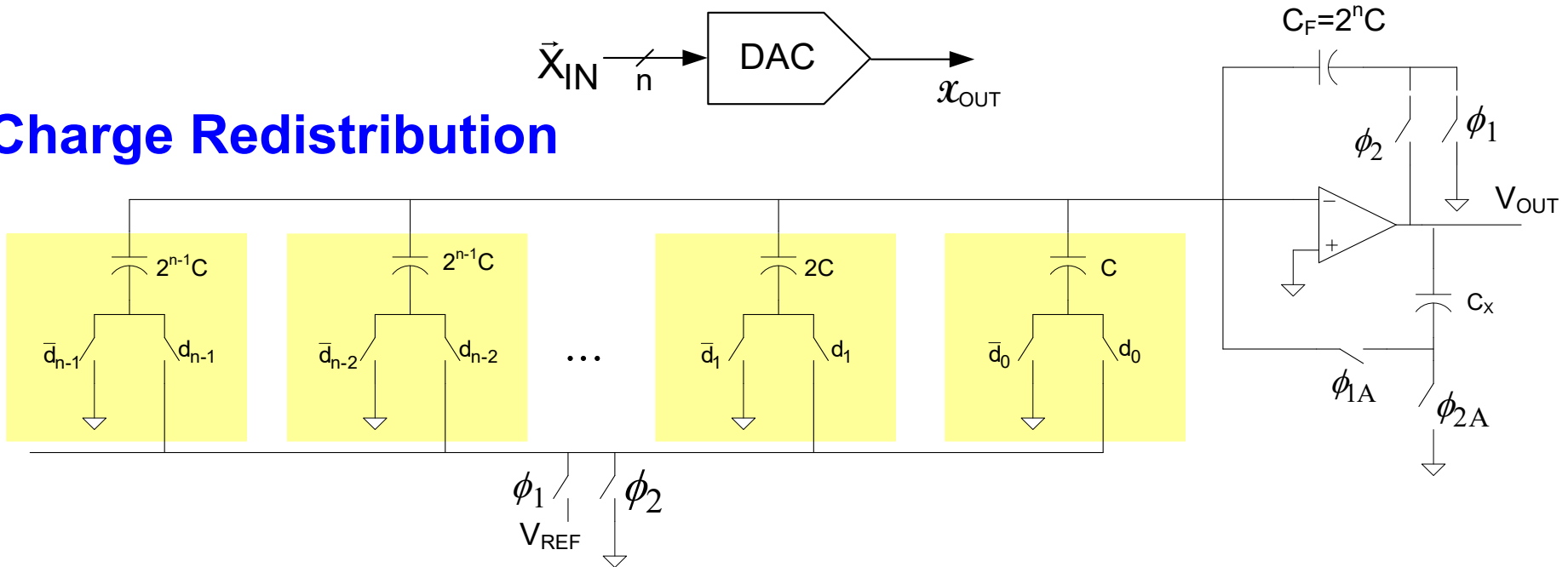


R-2R Resistor Arrays

# DAC Architectures



## Charge Redistribution



Unary cell used for capacitor array

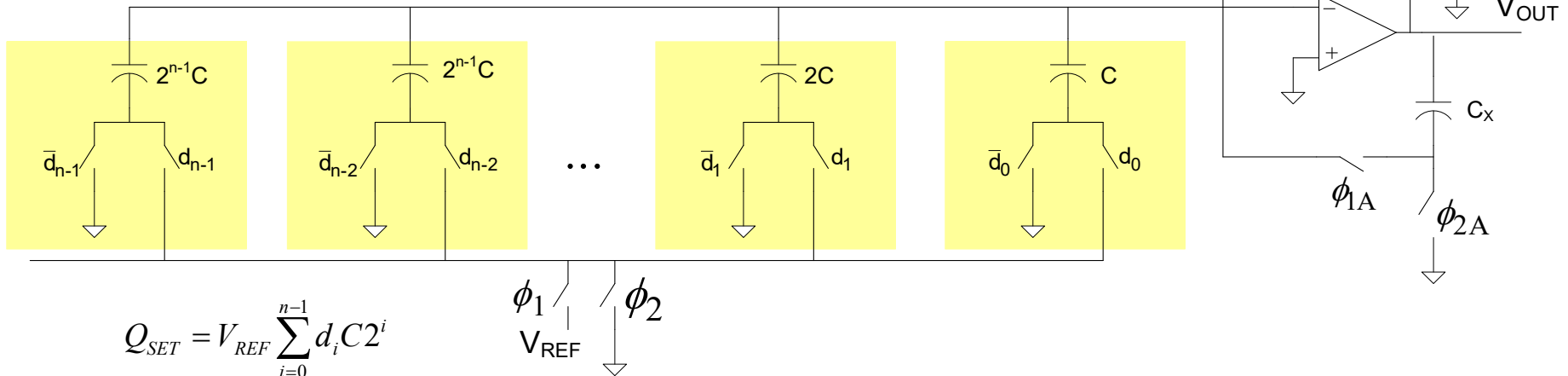
$C_x$  does some good things  
(mitigates  $V_{OS}$ ,  $1/f$  noise and finite gain errors)

Will not consider  $C_x$  affects at this time

# DAC Architectures



## Charge Redistribution



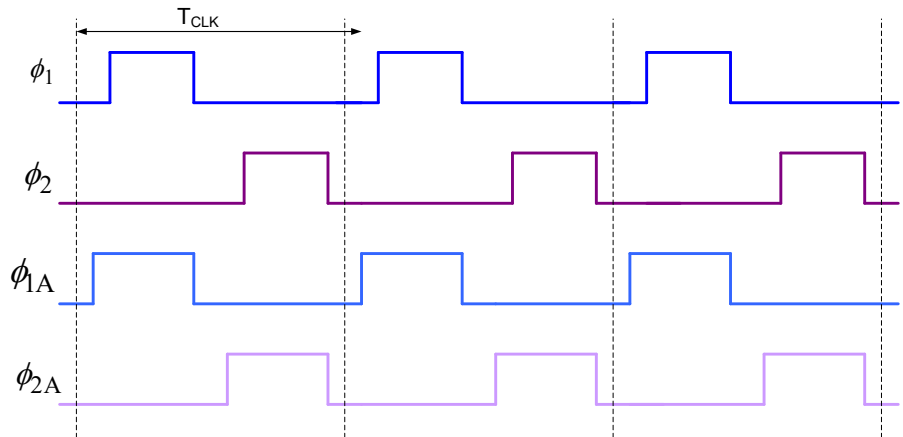
$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i C 2^i$$

$$Q_{RDIS} = V_{OUT} 2^n C$$

$$Q_{SET} = Q_{RDIS}$$

$$V_{REF} \sum_{i=0}^{n-1} d_i C 2^i = V_{OUT} 2^n C$$

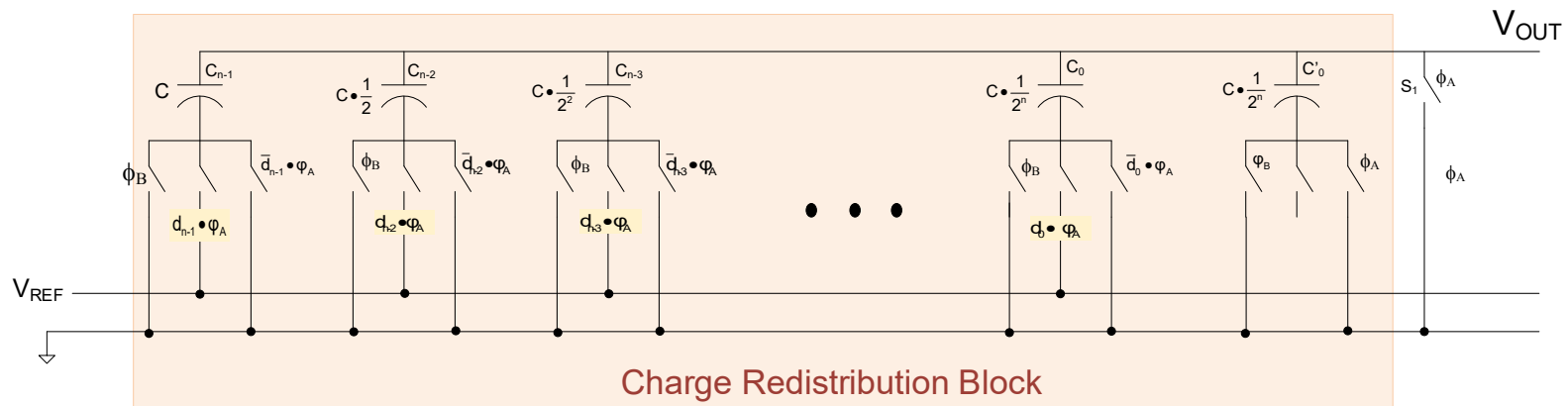
$$V_{OUT} = V_{REF} \sum_{i=0}^{n-1} d_i 2^{i-n}$$



Note capacitor values play no role in this analysis, only capacitor ratios

# DAC Architectures

## Charge Redistribution



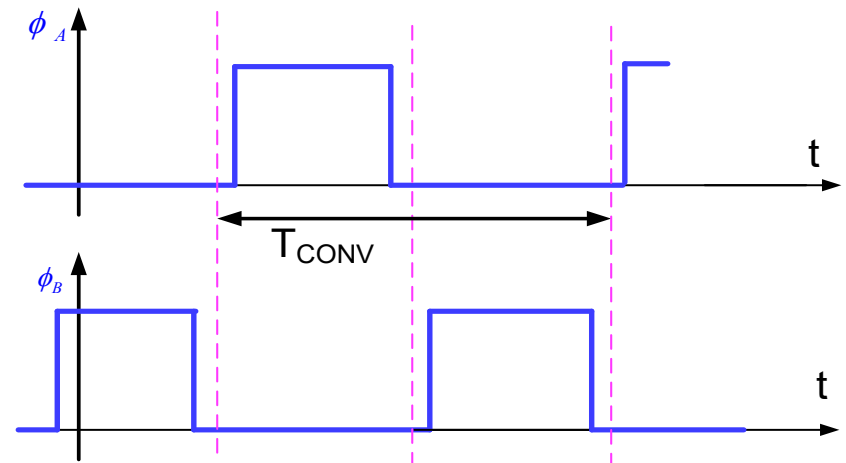
$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

$$Q_{DIS} = V_{OUT} \left( \sum_{i=0}^{n-1} C_i + [C'_0] \right) = V_{OUT} \left( \sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[ \frac{C}{2^n} \right] \right) = V_{OUT} C$$

$$Q_{SET} = Q_{DIS}$$

$$V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C$$

$$V_{OUT} = V_{REF} \sum_{i=0}^{n-1} d_i 2^{i-n}$$

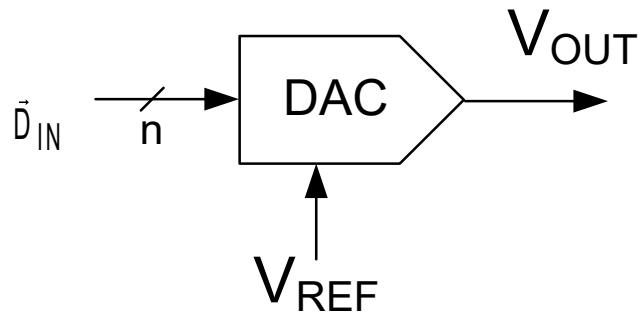


Note capacitor values play no role in this analysis, only capacitor ratios

# DAC Architectures

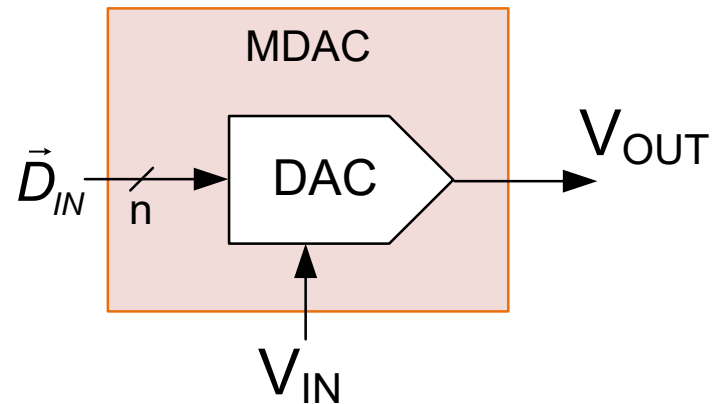


## MDAC (Multiplying DAC)



$V_{REF}$  fixed or limited range

$$V_{OUT} = V_{REF} \cdot [\vec{D}_{IN}]_{DECIMAL}$$



$V_{IN}$  Variable, often positive or negative

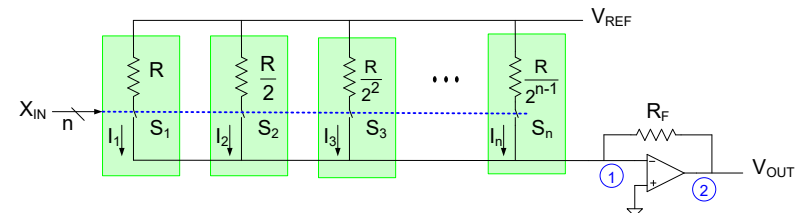
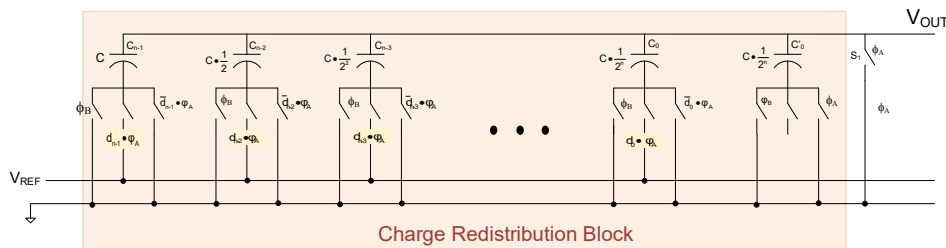
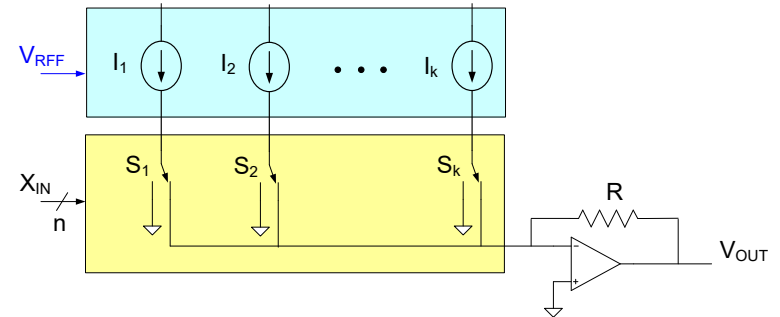
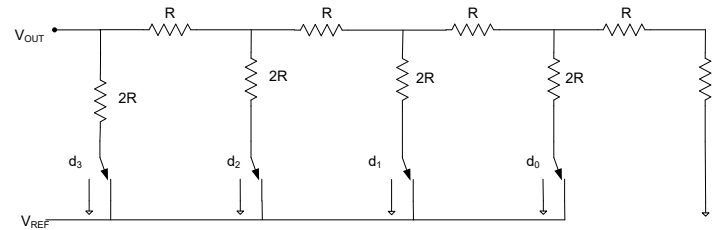
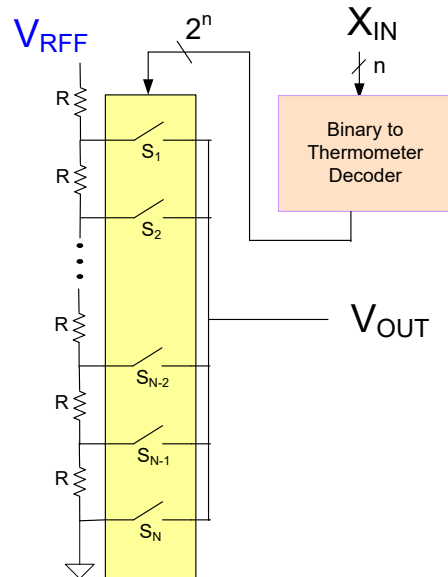
$$V_{OUT} = V_{IN} \cdot [\vec{D}_{IN}]_{DECIMAL}$$

- Some define MDACs to be DAC structures that have current outputs
- Many DAC structures can perform well as a MDAC (possibly one quadrant)
- Performance of some DAC structures limited if  $V_{REF}$  is varied

# DAC Architectures



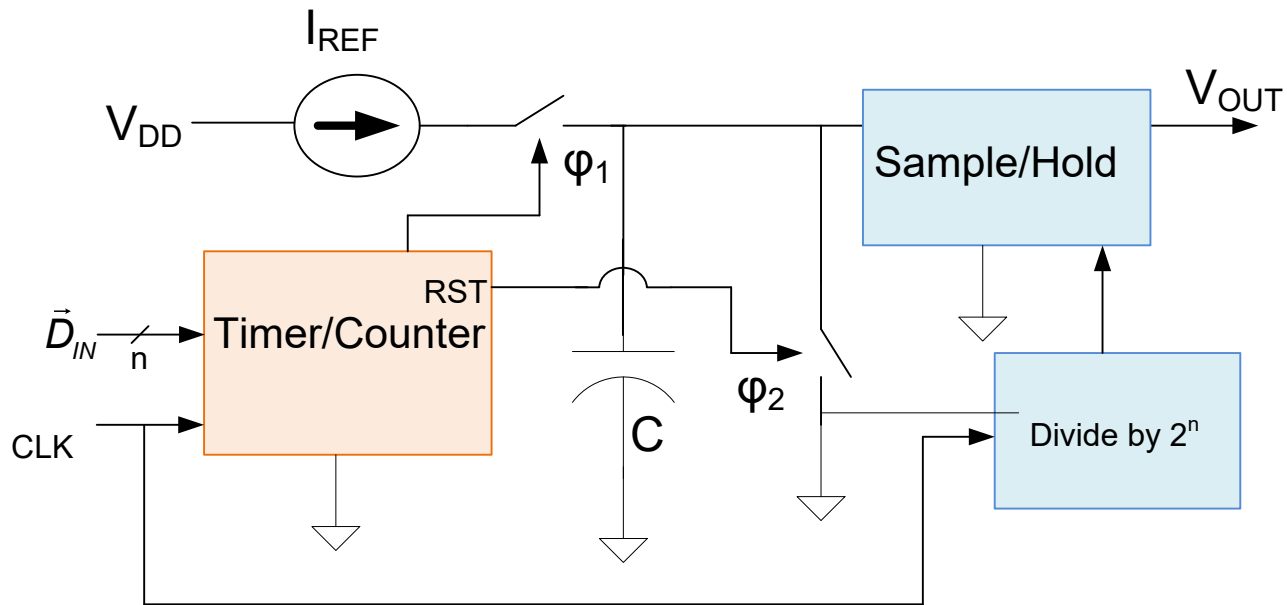
Suitable as MDAC?



# DAC Architectures



## Single Slope



Single-Slope DAC

Is this an MDAC?

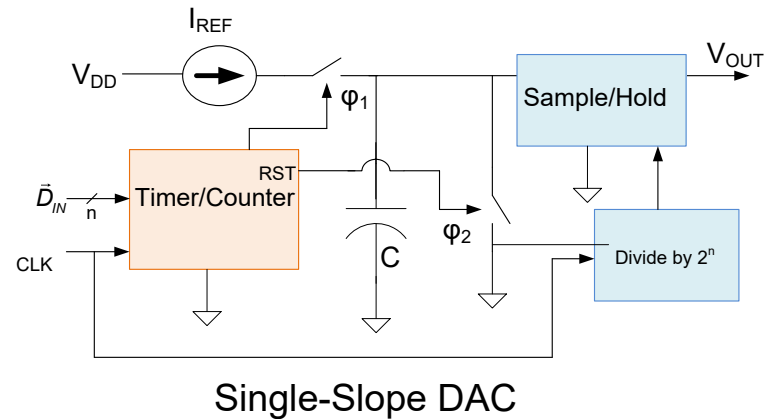
Yes – but multiplying factor is  $I_{REF}$



# DAC Architectures



## Single Slope



Can be viewed as a time-domain DAC where resolution headroom is very large

### Benefits of Single-Slope ADC?

- No matching required
- Very simple structure
- Mostly Digital
- Very low DNL
- Very fine resolution possible
- No previous code dependence
- No binary to thermometer decoder

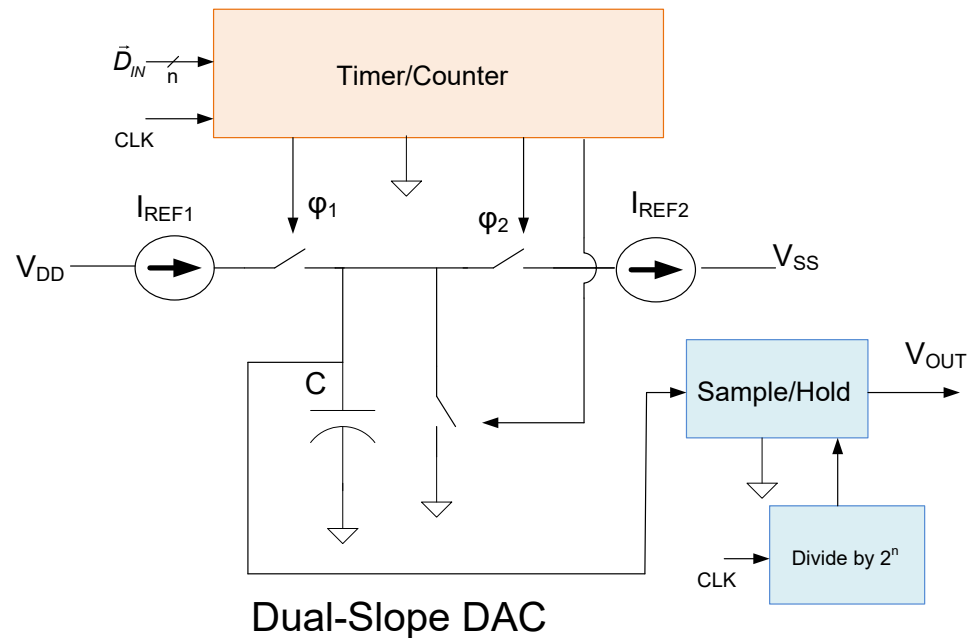
### Limitations of Single-Slope ADC?

- Slow conversion rate
- Large C
- Leakage currents that will be temperature dependent
- Nonlinearity in C?
- Nonlinearity in  $I_{REF}$

# DAC Architectures



## Dual Slope



Provides DAC with positive and negative outputs

Term “dual slope” means something different here than what we see in “dual slope” ADCs

Is this an MDAC?      Yes if  $I_{REF1} = I_{REF2} = I_{REF}$  but multiplying factor is  $I_{REF}$



Stay Safe and Stay Healthy !

**End of Lecture 12**